Claims:

Sub B1

An SCM modulator, comprising:

an input interface for receiving one or more time-discrete samples of a signal; and

an SCM Mapper circuit that converts the aggregate of the one or more time-discrete samples to analog and digital output symbols representing a mix of analog and digital values, wherein said analog output symbols represent amplitude values of a selected subspace of a stretched transformation of said aggregated input signals and said digital output symbols represent an indication of the subspaces chosen in the stretched transformation.

2. The SCM modulator of Claim 1, wherein said SCM Mapper circuit further comprises a stretching transformation circuit for mapping the one or more of said signal samples onto a transformed signal space represented by an aggregate of one or more transformed signals and a subspace slicer that selects one or more subspaces from said transformed signal space and outputs said mix of analog and digital symbols based on the selecting subspace and the transformed signal samples.

3. The SCM modulator of Claim 1 further comprising means for forward error correcting said digital output symbols before transmission.

4. The SCM modulator of claim 2, wherein said stretching transformation circuit further comprises a linear expansion circuit for linearly expanding the sample signals in one or more dimensions of said input signals space.

5. The SCM modulator of claim 2, wherein said stretching transformation circuit further comprises a non-linear expansion circuit that transforms a quarter-circle sub space onto a full circle transformed signal space.

6. The SCM modulator of claim 2, wherein said stretching transformation circuit further comprises conformal mapping.

7. The SCM modulator of claim 1 further comprising a multiplexer for multiplexing the analog and digital symbols for transmission over a common communications channel.

8. The SCM modulator of claim 7, further comprising an SCM Mapper comprising means for pairing said multiplexed symbols and a quadrature amplitude modulator for quadrature amplitude modulating each pair of signals to generate QAM signals.

9. The SCM modulator of Claim 8, wherein each of the QAM signals comprise analog symbols or digital symbols as originated from the output of said SCM Mapper.

10. The SCM modulator of Claim 9, wherein the QAM signals comprise a mix of both analog and digital symbols as originated from the output of said SCM Mapper.

11. An SCM demodulator, comprising:

an input interface for receiving one or more analog and digital symbols, the analog symbols representing an amplitude of values of a selected subspace of a stretched transformation of an input signal and said digital symbols represent an indication of the subspaces chosen in the stretched transformation; and

an SCM Demapper circuit that converts the received analog and digital signals into an aggregate of one or more samples of a signal, each sample generated based on a combination of an analog symbol and a digital symbol.

12. The SCM demodulator of Claim 11, wherein said SCM Demapper circuit further comprises a subspace positioner that positions a received analog and digital symbols onto the an

aggregate signal space based on the digital symbol and an inverse transformation circuit that compresses the aggregate signal space and generates a demodulated signal.

13. The SCM demodulator of Claim 12 further comprises a forward error decoder that decodes the digital symbols prior to the subspace positioner.

14. The SCM demodulator of Claim 12, wherein said inverse transformation comprises a linear contraction in one or more dimensions of said received signals space.

15. The SCM demodulator of claims 11 further comprising an SCM Demapper further comprises a demultiplexer for demultiplexing the analog and digital symbols that are multiplexed for transmission over a common communications channel.

16. The SCM demodulator of claim 15, wherein said SCM demapper further comprises means for depairing said multiplexed symbols and means for demodulating the multiplexed signal using quadrature amplitude demodulation to generate .

17. The demodulator of Claim 16, wherein each quadrature amplitude demodulated pair of symbol comprise either analog or digital symbols.

18. The demodulator of Claim 16, wherein each quadrature amplitude demodulated pair of symbol comprise a mix of both analog and digital symbols.